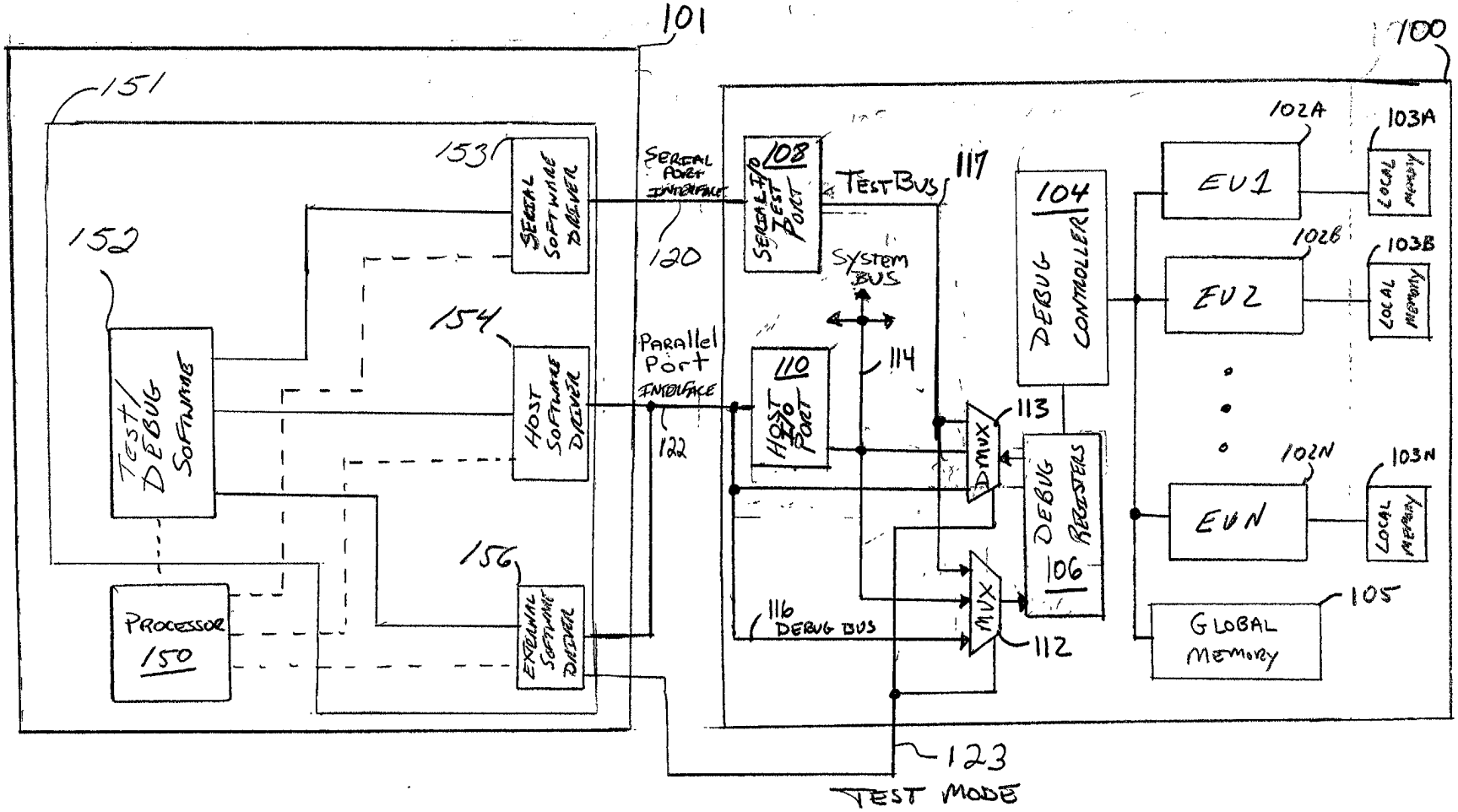
101
100
151
153
SERIAL SOFTWARE DRIVER
152
TEST/DEBUG SOFTWARE
154
HOST SOFTWARE DRIVER
156
EXTERNAL SOFTWARE DRIVER
PROCESSOR 150
SERIAL PORT INTERFACE
120
PARALLEL PORT INTERFACE
122
108
SERIAL I/O TEST PORT
110
HOST I/O PORT
TEST BUS
117
SYSTEM BUS
114
116
DEBUG BUS
DMUX
113
MUX
112
104
DEBUG CONTROLLER
DEBUG REGISTERS
106
102A
EU1
103A
LOCAL MEMORY
102B
EU2
103B
LOCAL MEMORY
102N
EUN
103N
LOCAL MEMORY
GLOBAL MEMORY
105
123
TEST MODE

FIG. 1A

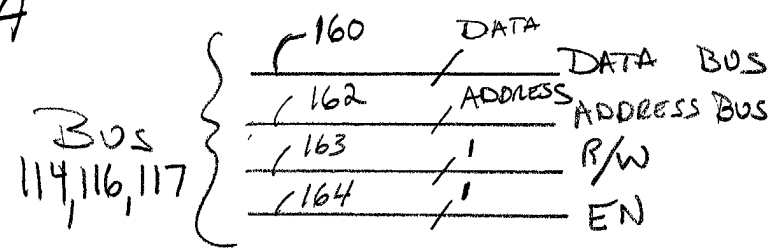
BUS 114, 116, 117
160
DATA
DATA BUS
162
ADDRESS
ADDRESS BUS
163
1
R/W
164
1
EN

FIG. 1B

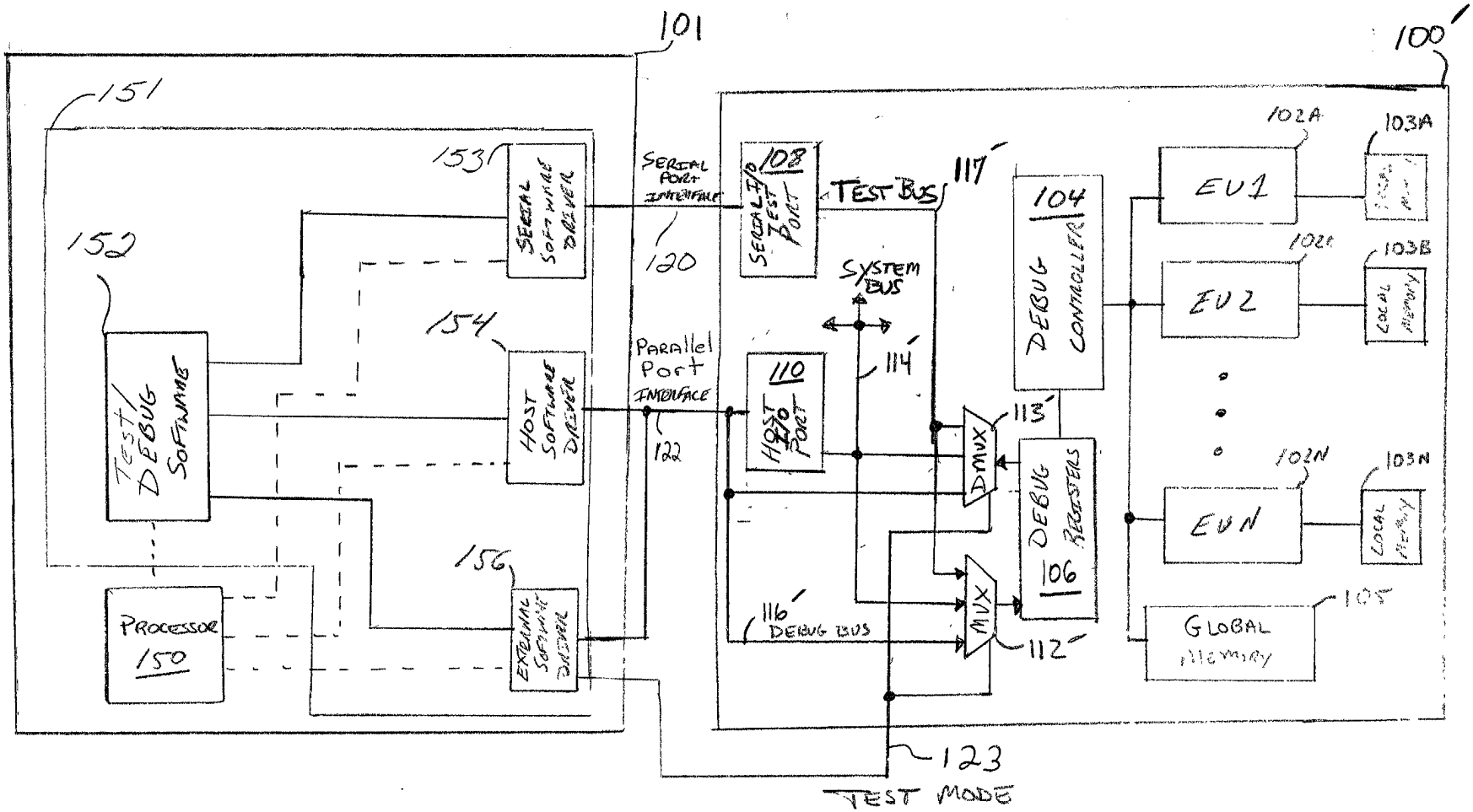
101
100
151
153
152
154
156
SERIAL SOFTWARE DRIVER
HOST SOFTWARE DRIVER
EXTERNAL SOFTWARE DRIVER
TEST/DEBUG SOFTWARE
PROCESSOR 150
SERIAL PORT INTERFACE
120
PARALLEL PORT INTERFACE
122
108
SERIAL I/O TEST PORT
110
HOST I/O PORT
TEST BUS
117
SYSTEM BUS
114
116
DEBUG BUS
104
DEBUG CONTROLLER
106
DEBUG REGISTERS
113
DMUX
MUX
112
102A
EU1
103A
102B
EU2
103B
LOCAL MEMORY
102N
EUN
103N
105
GLOBAL MEMORY
123
TEST MODE

FIG. 1C

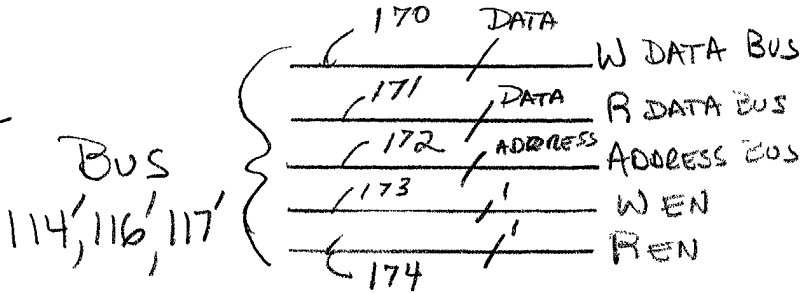
170
DATA
W DATA BUS
171
DATA
R DATA BUS
172
ADDRESS
ADDRESS BUS
173
1
W EN
1
R EN
174
BUS 114, 116, 117

FIG. 1D

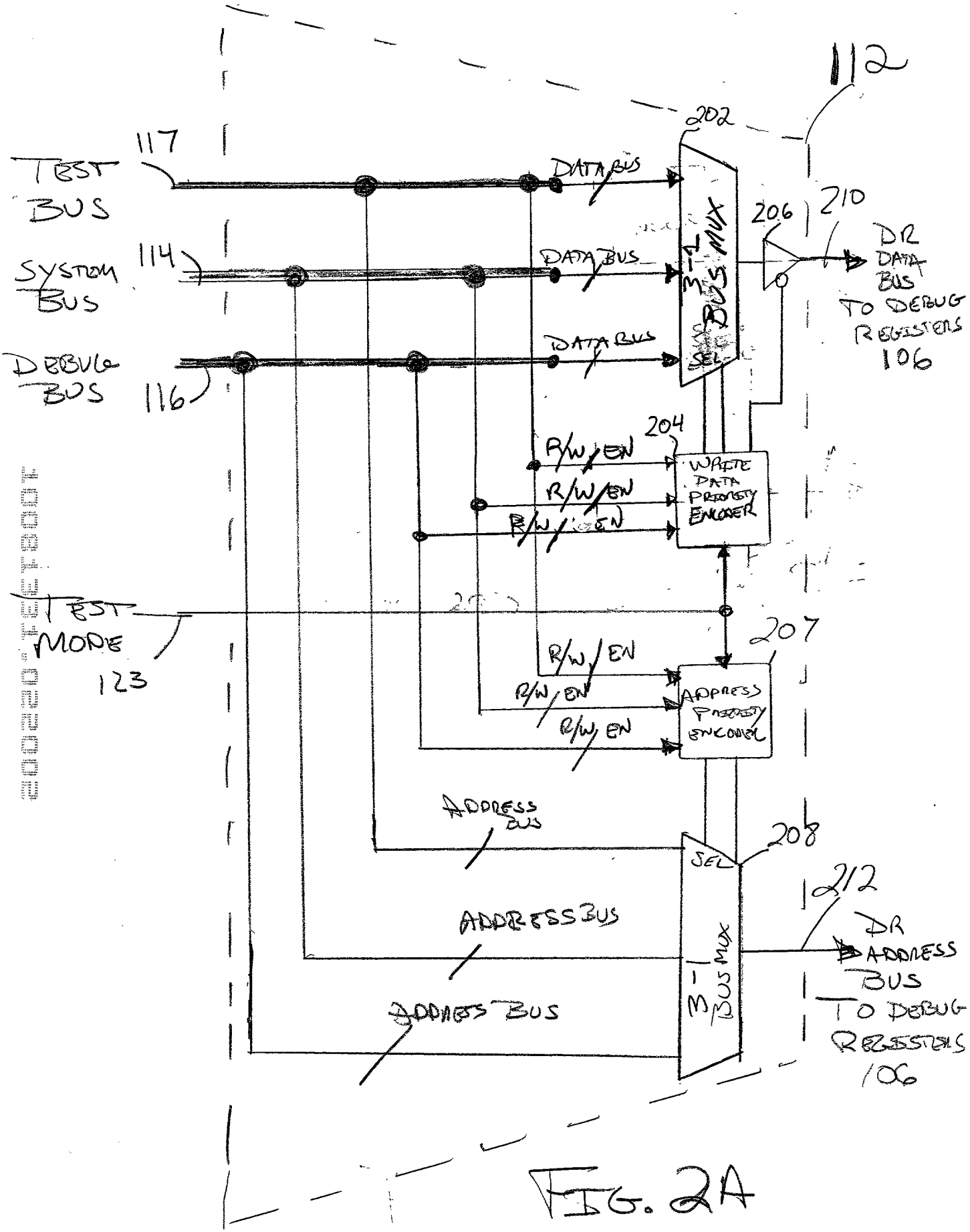
112
202
117
TEST BUS
DATA BUS
114
SYSTEM BUS
DATA BUS
DEBUG BUS
116
DATA BUS
M-1 BUS MUX
SEL
206
210
DR DATA BUS TO DEBUG REGISTERS 106
204
R/W EN
R/W EN
R/W EN
WRITE DATA PRIORITY ENCODER
TEST MODE
123
207
R/W EN
R/W EN
R/W EN
ADDRESS PRIORITY ENCODER
ADDRESS BUS
208
SEL
212
M-1 BUS MUX
ADDRESS BUS
ADDRESS BUS
DR ADDRESS BUS TO DEBUG REGISTERS 106

FIG. 2A

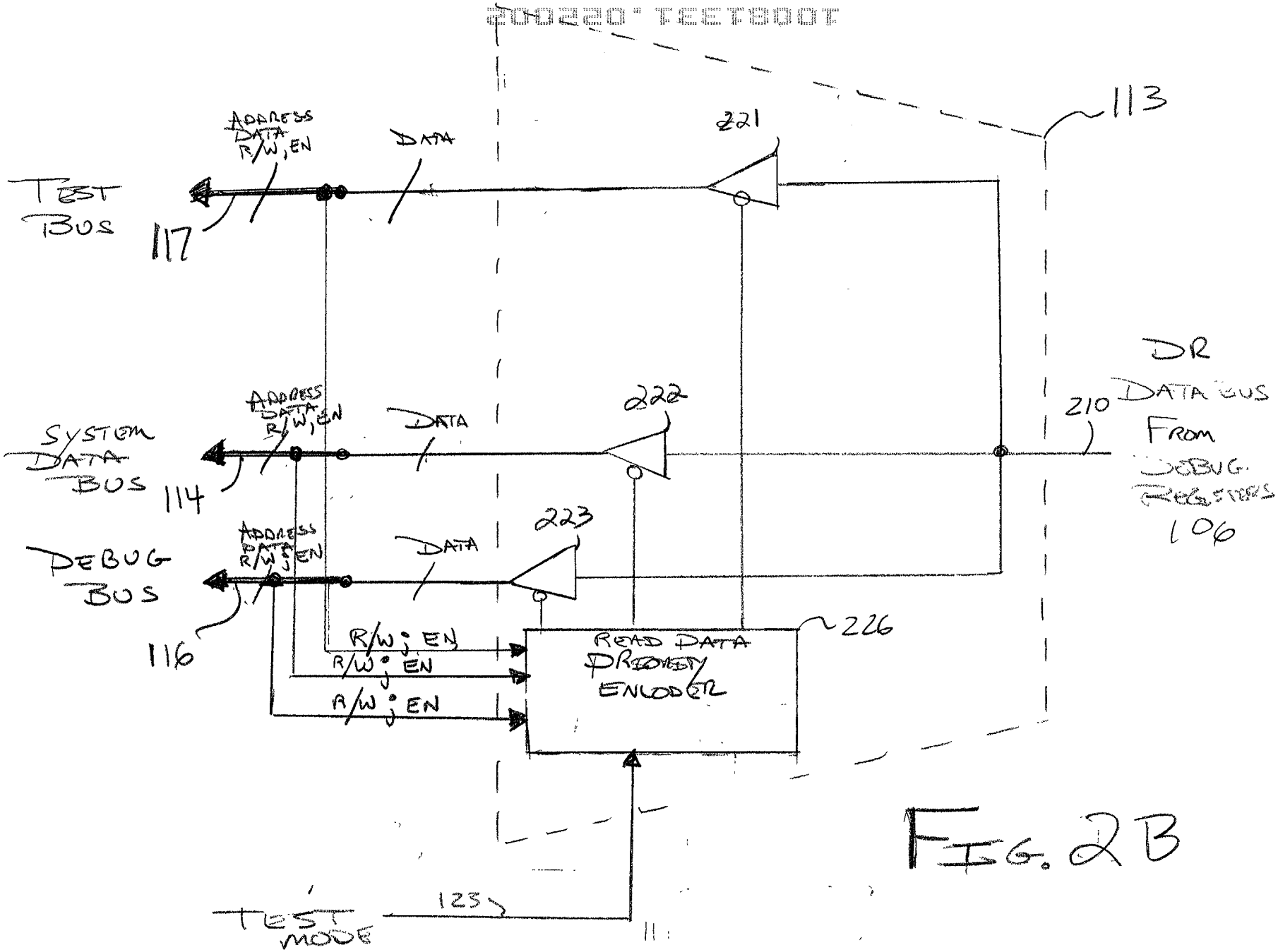
TEST BUS
117
ADDRESS DATA R/W, EN
DATA
221
113
SYSTEM DATA BUS
114
222
210
DR DATA BUS FROM DEBUG REGISTERS 106
DEBUG BUS
116
223
R/W, EN
R/W, EN
R/W, EN
READ DATA PRIORITY ENCODER
226
TEST MODE
123

FIG. 2B

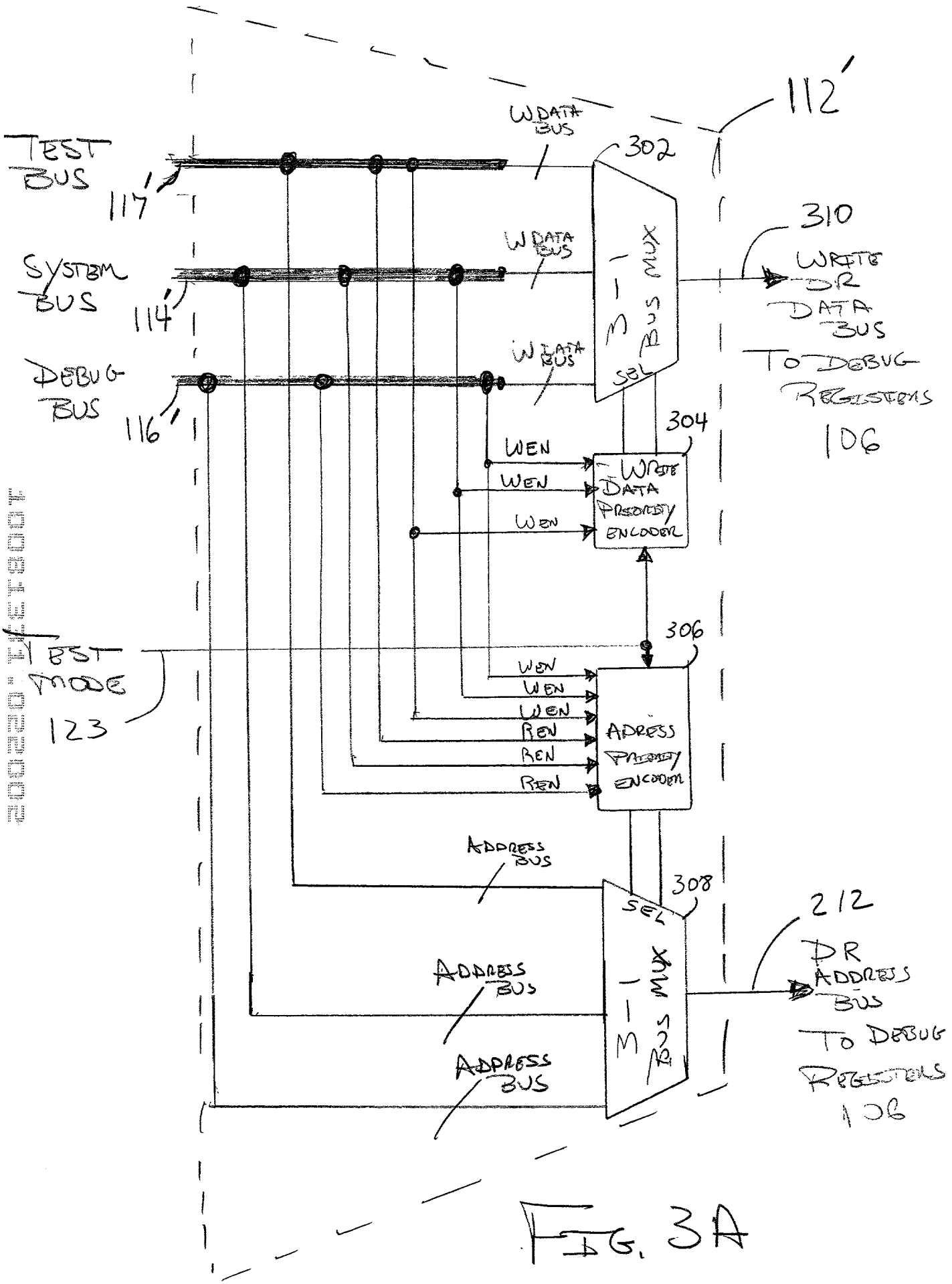
112'
TEST BUS
117'
SYSTEM BUS
114'
DEBUG BUS
116'
W DATA BUS
W DATA BUS
W DATA BUS
302
2 - 1 MUX
SEL
310
WRITE DR DATA BUS
TO DEBUG REGISTERS
106
304
WEN
WEN
WEN
WRITE DATA PRIORITY ENCODER
306
TEST MODE
123
WEN
WEN
WEN
REN
REN
REN
ADDRESS PRIORITY ENCODER
ADDRESS BUS
308
SEL
2 - 1 MUX
212
DR ADDRESS BUS
TO DEBUG REGISTERS
106
ADDRESS BUS
ADDRESS BUS

FIG. 3A

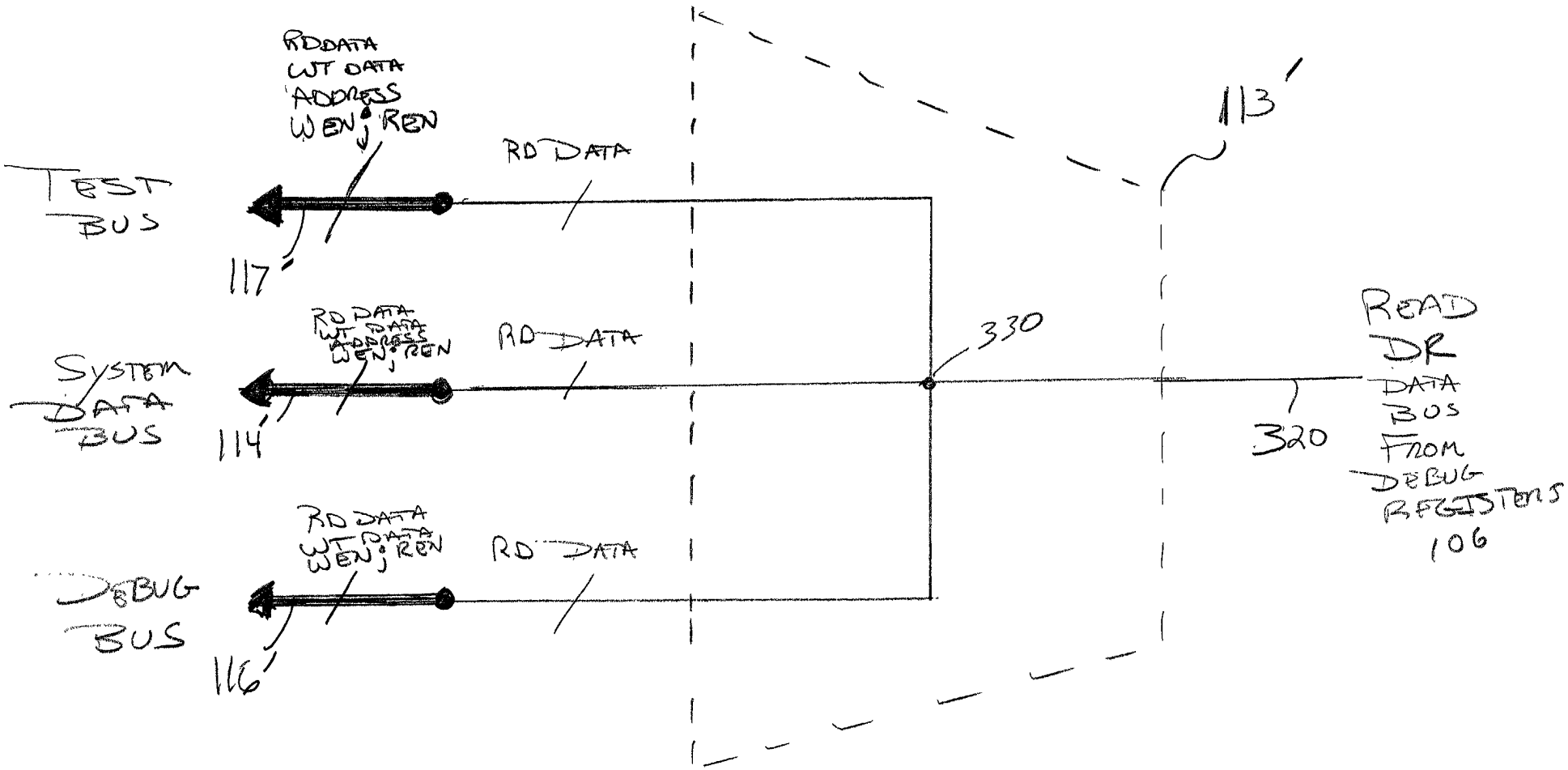
RDDATA
WT DATA
ADDRESS
WEN
REN
TEST BUS
RD DATA
117
113
RD DATA
WT DATA
ADDRESS
WEN
REN
SYSTEM DATA BUS
RD DATA
114
330
READ DR DATA BUS FROM DEBUG REGISTERS 106
320
RD DATA
WT DATA
WEN
REN
DEBUG BUS
RD DATA
116

FIG. 3B

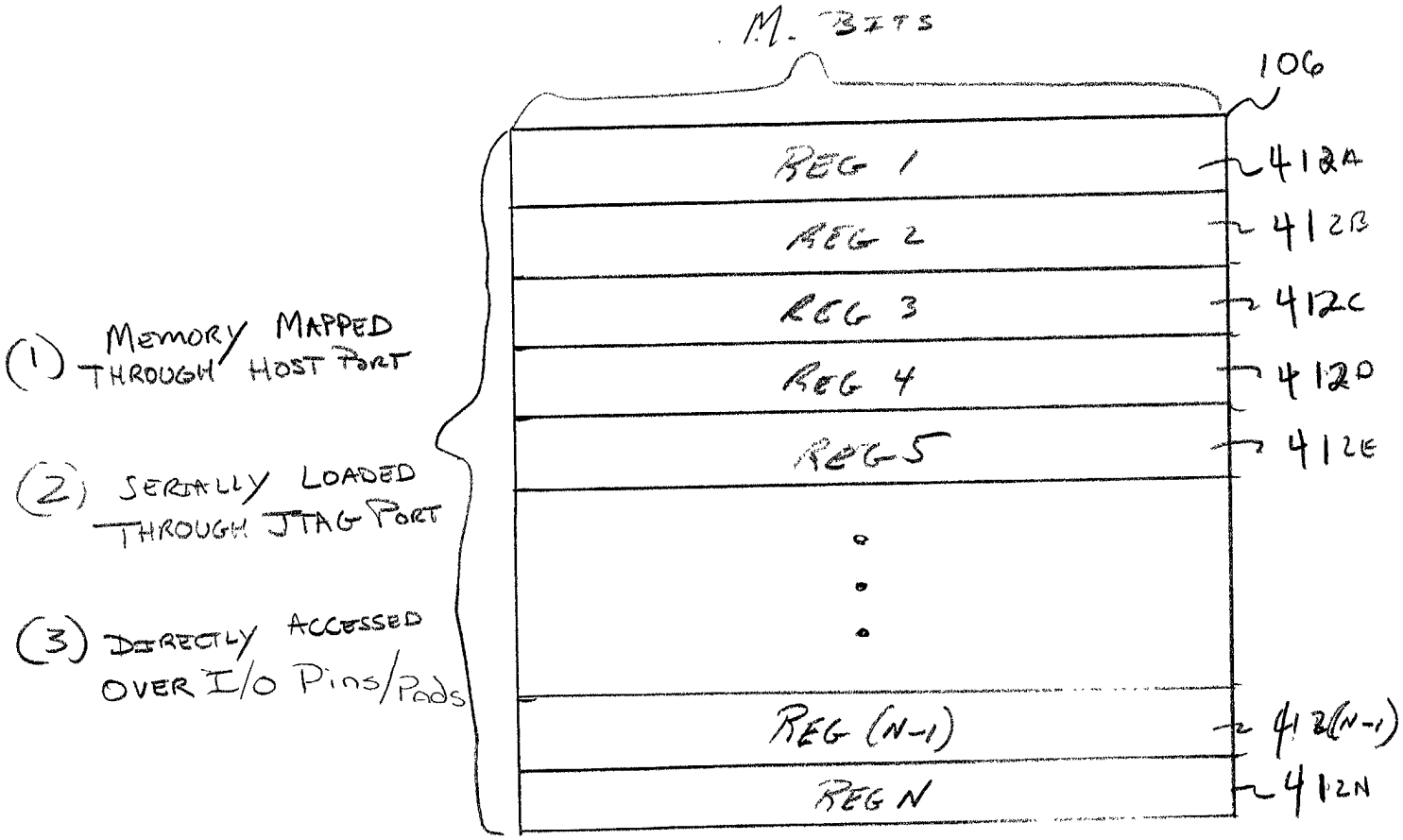
M. BITS
106
REG 1
412A
REG 2
412B
REG 3
412C
REG 4
412D
REG 5
412E
REG (N-1)
412(N-1)
REG N
412N
(1) MEMORY MAPPED THROUGH HOST PORT
(2) SERIALLY LOADED THROUGH JTAG PORT
(3) DIRECTLY ACCESSED OVER I/O Pins/Pads

FIG. 4

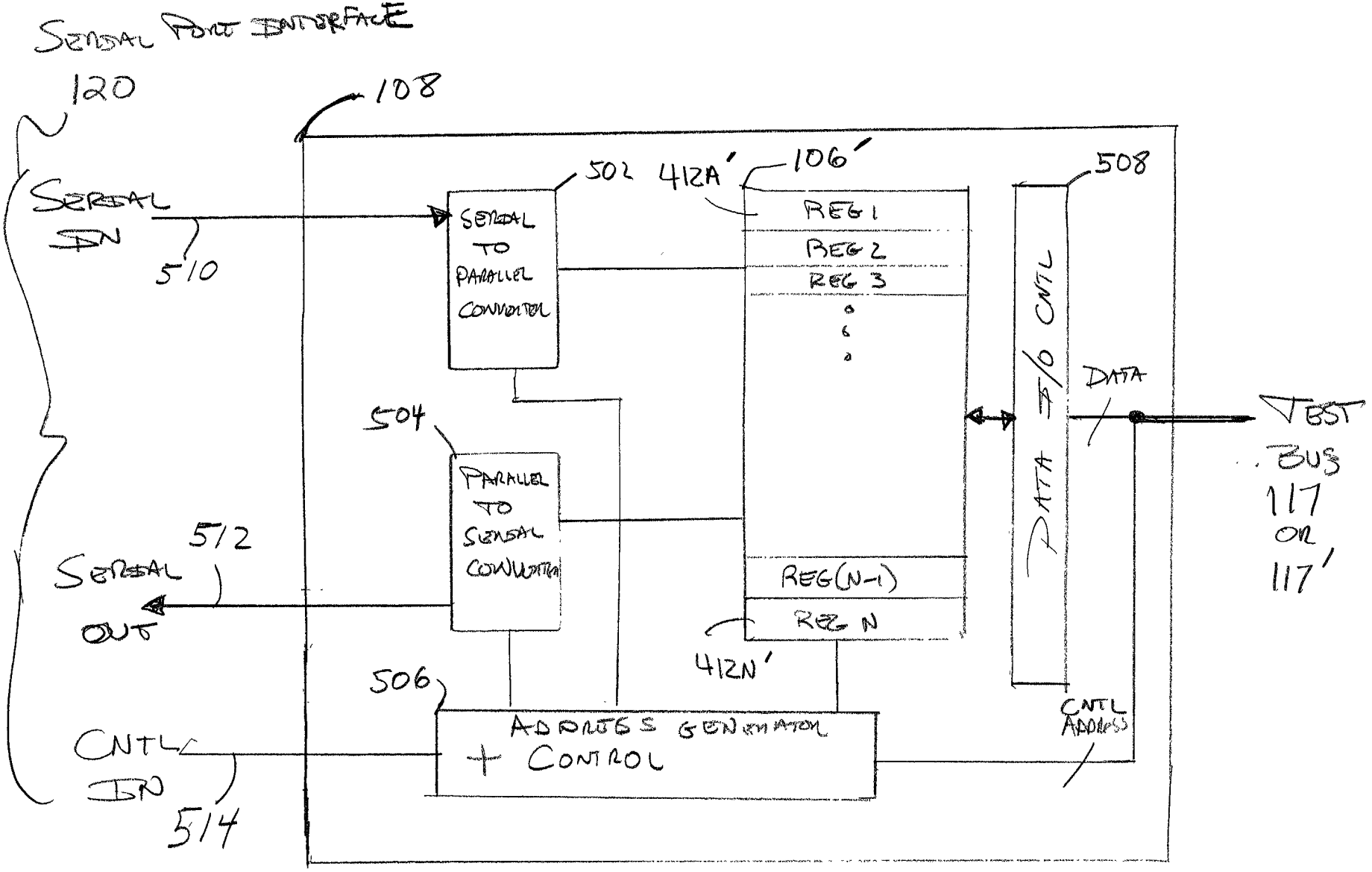
SERIAL PORT INTERFACE
120
108
SERIAL IN
510
502
SERIAL TO PARALLEL CONVERTER
412A'
106'
REG 1
REG 2
REG 3
REG (N-1)
REG N
412N'
508
I/O CNTL
DATA
DATA
TEST BUS 117 OR 117'
504
PARALLEL TO SERIAL CONVERTER
512
SERIAL OUT
506
ADDRESS GENERATION + CONTROL
CNTL ADDRESS
CNTL IN
514

FIG. 5

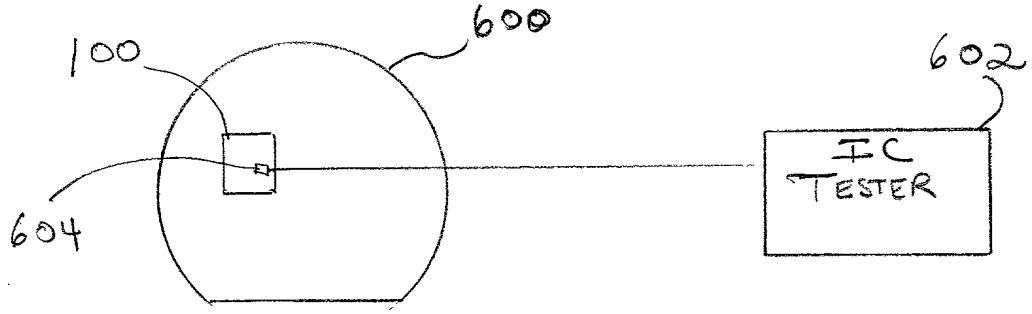

FIG. 6A

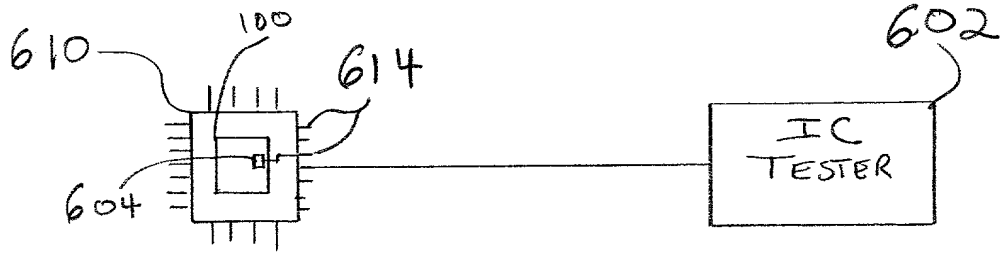

FIG. 6B

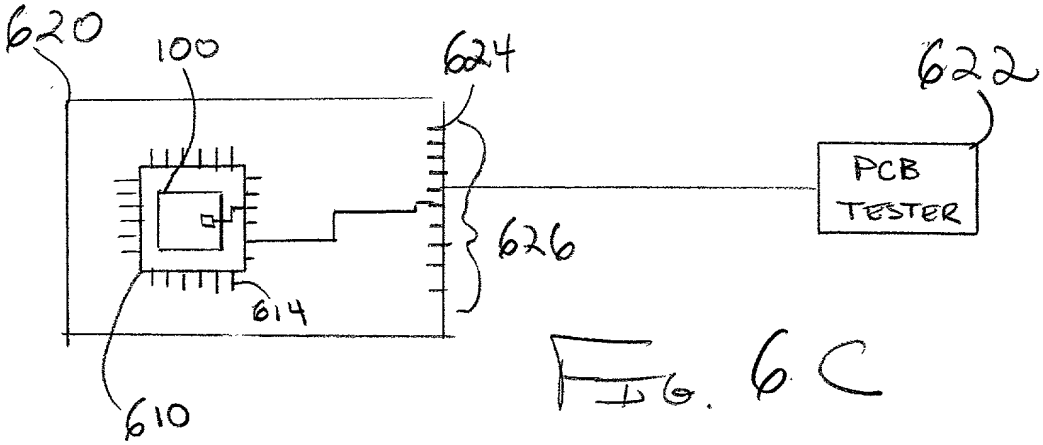

FIG. 6C

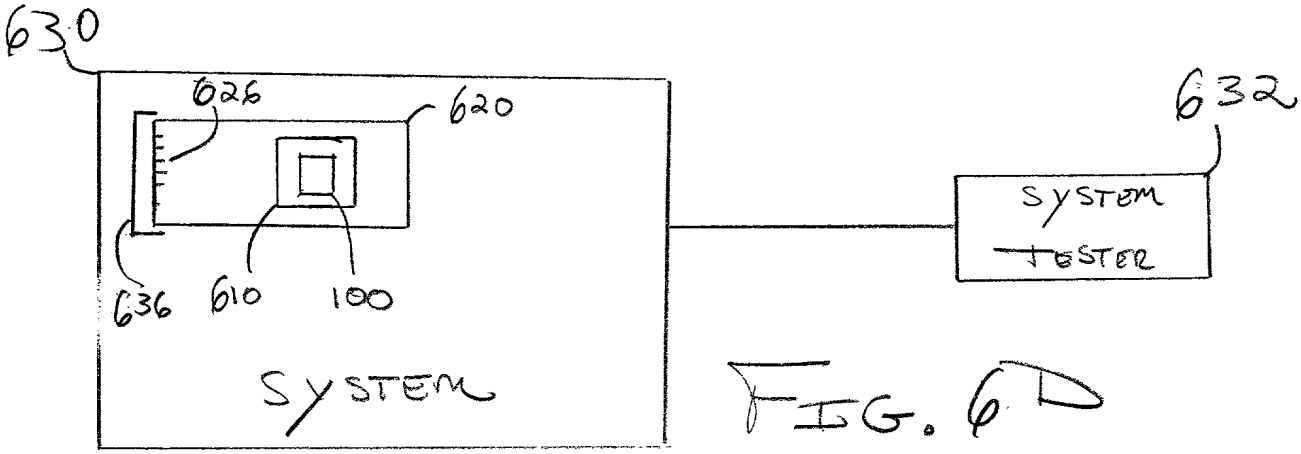

FIG. 6D